INTEGRATED CIRCUITS

DATA SHEET

TDA1547
Dual top-performance bitstream DAC

Product specification
File under Integrated Circuits, IC01

September 1991

Philips
Semiconductors

PHILIPS

FEATURES

BITSTREAM CONVERSION

- Top-grade audio performance
  - very low harmonic distortion
  - high signal-to-noise ratio
  - wide dynamic range of approximately 108 dB (not A-weighted)
- High crosstalk immunity
- Bitstream concept
  - high over-sampling rate up to 192 f_s
  - pulse-density modulation
  - inherently monotonic
  - no zero-crossing distortion

GENERAL DESCRIPTION

The TDA1547 is a dedicated one-bit digital-to-analog converter to facilitate a high fidelity sound reproduction of digital audio. The TDA1547 is extremely suitable for use in high quality audio systems such as Compact Disc and DAT players, or in digital amplifiers and digital signal processing systems. The TDA1547 is used in combination with the SAA7350 bitstream circuit, which includes the third-order noise shaper. The excellent performance of the SAA7350 and TDA1547 bitstream conversion system is obtained by separating the noise shaping circuit and the one-bit conversion circuit over two IC's, thereby reducing the crosstalk between the digital and analog parts. The TDA1547 one-bit converter is processed in BIMOS. In the digital logic and drivers bipolar transistors are used to optimize speed and to reduce digital noise generation. In the analog part the bipolar transistors are used to obtain high performance of the operational amplifiers. Special layout precautions have been taken to achieve a high crosstalk immunity. The layout of the TDA1547 has fully separated left and right channels and supply voltage lines between the digital and analog sections.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1547[(1)]	32	SDIL	plastic	SOT232A

Note

1. SOT-232-1; 1996 August 23.

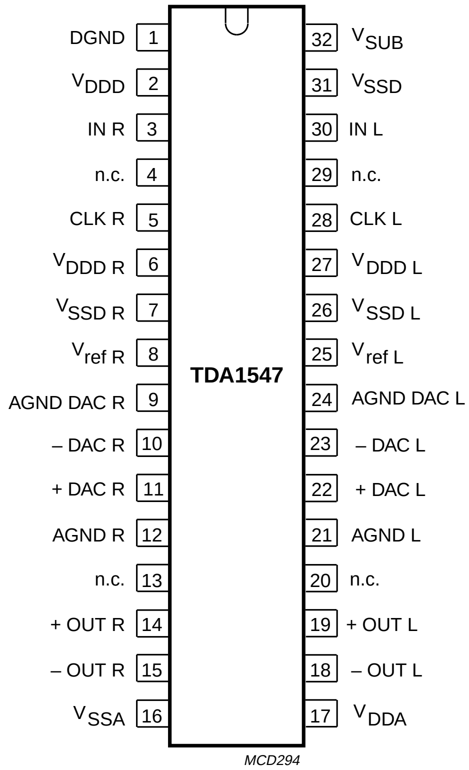


Fig.1 Pinning diagram.

Dual top-performance bitstream DAC TDA1547

PINNING

SYMBOL	PIN	DESCRIPTION
DGND	1	0 V digital supply
V_{DDD}	2	5 V digital supply for both channels
IN R	3	serial one-bit data input for the right channel
n.c.	4	pin not connected; should preferably be connected to digital ground
CLK R	5	clock input for the right channel
$V_{DDD\ R}$	6	5 V digital supply for the right channel; this voltage determines the internal logic HIGH level in the right channel
$V_{SSD\ R}$	7	–3.5 V digital supply for the right channel; this voltage determines the internal logic LOW level in the right channel
$V_{ref\ R}$	8	–4 V reference voltage for the right channel switched capacitor DAC
AGND DAC R	9	0 V reference voltage for the right channel switched capacitor DAC; this pin should be connected to analog ground
–DAC R	10	output from the right negative switched capacitor DAC; feedback connection for the right negative operational amplifier
+DAC R	11	output from the right positive switched capacitor DAC; feedback connection for the right positive operational amplifier
AGND R	12	0 V reference voltage for both right channel operational amplifiers
n.c.	13	pin not connected; should preferably be connected to analog ground
+OUT R	14	+ output of the switched capacitor operational amplifier
–OUT R	15	– output of the switched capacitor operational amplifier
V_{SSA}	16	–5 V analog supply
V_{DDA}	17	5 V analog supply
–OUT L	18	– output of the switched capacitor operational amplifier
+OUT L	19	+ output of the switched capacitor operational amplifier
n.c.	20	pin not connected; should preferably be connected to analog ground
AGND L	21	0 V reference voltage for both left channel operational amplifiers
+DAC L	22	output from the left positive switched capacitor DAC; feedback connection for the left positive operational amplifier
–DAC L	23	output from the left negative switched capacitor DAC; feedback connection for left negative operational amplifier
AGND DAC L	24	0 V reference voltage for the left channel switched capacitor DAC; this pin should be connected to analog ground
$V_{ref\ L}$	25	–4 V reference voltage for the left channel switched capacitor DAC
$V_{SSD\ L}$	26	–3.5 V digital supply for the left channel; this voltage determines the internal logic LOW level in the left channel
$V_{DDD\ L}$	27	5 V digital supply for the left channel; this voltage determines the internal logic HIGH level in the left channel

SYMBOL	PIN	DESCRIPTION
CLK L	28	clock input for the left channel
n.c.	29	pin not connected; should preferably be connected to digital ground
IN L	30	serial one-bit data input for the left channel
V_{SSD}	31	–5 V digital supply for both channels
V_{SUB}	32	–5 V substrate voltage

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Supply voltages						
$V_{DDD\ L.\ R}$	positive digital supply voltage for one channel; pins 27 and 6		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage for both channels; pin 2		4.5	5.0	5.5	V
$V_{SSD\ L.\ R}$	negative digital supply voltage for one channel; pins 26 and 7		–4.0	–3.5	–3.0	V
V_{SSD}	negative digital supply voltage for both channels; pin 31		–5.5	–5.0	–4.5	V
V_{DDA}	positive analog supply voltage; pin 17		4.5	5.0	6	V
V_{SSA}	negative analog supply voltage; pin 16		–6.0	–5.0	–4.5	V
Supply current						
$I_{DDD\ L.\ R}$	positive digital supply current for one channel; pins 27 and 6		–	0.1	–	mA
I_{DDD}	digital supply current for both channels; pin 2		–	29.0	–	mA
$I_{SSD\ L.\ R}$	negative digital supply current for one channel; pins 26 and 7		–	–0.1	–	mA
I_{SSD}	negative supply current for both channels; pin 31		–	–28.0	–	mA
I_{DDA}	positive analog supply current; pin 17		–	51.0	–	mA
I_{SSA}	negative analog supply current; pin 16		–	–51.0	–	mA
P_{tot}	total power dissipation		–	800	–	mW
$V_{OUT(RMS)}$	output voltage (RMS value)	f_{CLK} = 8.46 MHz; notes 1 and 2	0.85	1.0	1.15	V

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Supply current						
(THD + N)/S	THD + Noise; 0 dB	1 kHz; notes 2 and 3	–	–101	–96	dB
			–	0.0009	0.0016	%
(THD + N)/S	THD + Noise; 0 dB	f = 20 Hz to 20 kHz;	–	–101	-	dB
		notes 2 and 4	–	0.0009	-	%
(THD + N)/S	THD + Noise; –20 dB	f = 1 kHz; notes 2 and 3	–	–88	–84	dB
(THD + N)/S	THD + Noise; –60 dB	f = 1 kHz; notes 2 and 3	–	–48	–44	dB
S/N	signal-to-noise ratio	pattern 0101..; notes 2 and 5	109	111	–	dB
S/N	signal-to-noise ratio; “A”-weighting	pattern 0101..; notes 2 and 5	–	113	–	dB
f_{CLK}	maximum clock frequency		–	–	10	MHz
α	channel separation	f = 1 kHz	101	115	–	dB
T_{amb}	operating ambient temperature		–20	–	70	°C

Notes to the quick reference data

1. Output level tracks linearly with both the clock frequency and the reference voltage ($V_{ref\ L}$ or $V_{ref\ R}$).
2. Device measured in differential mode with external components as shown in Fig.5.
3. Measured with a one-bit data signal generated by the SAA7350 from an 8 f_S (352.8 kHz), 20-bit, 1 kHz digital sinewave. Measured over a 20 Hz to 20 kHz bandwidth.
4. Measured with a one-bit data signal generated by the SAA7350 from an 8 f_S (352.8 kHz), 20-bit, 20 Hz to 20 kHz digital sinewave. Measured over a 20 Hz to 20 kHz bandwidth.
5. The specified signal-to-noise ratio includes noise introduced by the application components as shown in Fig.5.

FUNCTIONAL DESCRIPTION

Both channels are completely separated to reach the desired high crosstalk suppression level.
Each channel consists of the following functional parts:

– One-bit input, which latches the incoming data to the system clock.
– Switch driver circuit, which generates the non-overlapping clock- and data-signals that control the DAC switched capacitor networks.
– Switched capacitor network, this forms the actual DAC function, it supplies charge packets to the low-pass filter, under control of the incoming one-bit code.
– Two high performance operational amplifiers, that perform the charge packet to voltage conversion and deliver a differential output signal. The first pole of the low-pass filter is built around them.

THERMAL RESISTANCE

SYMBOL	PARAMETER	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	60	K/W

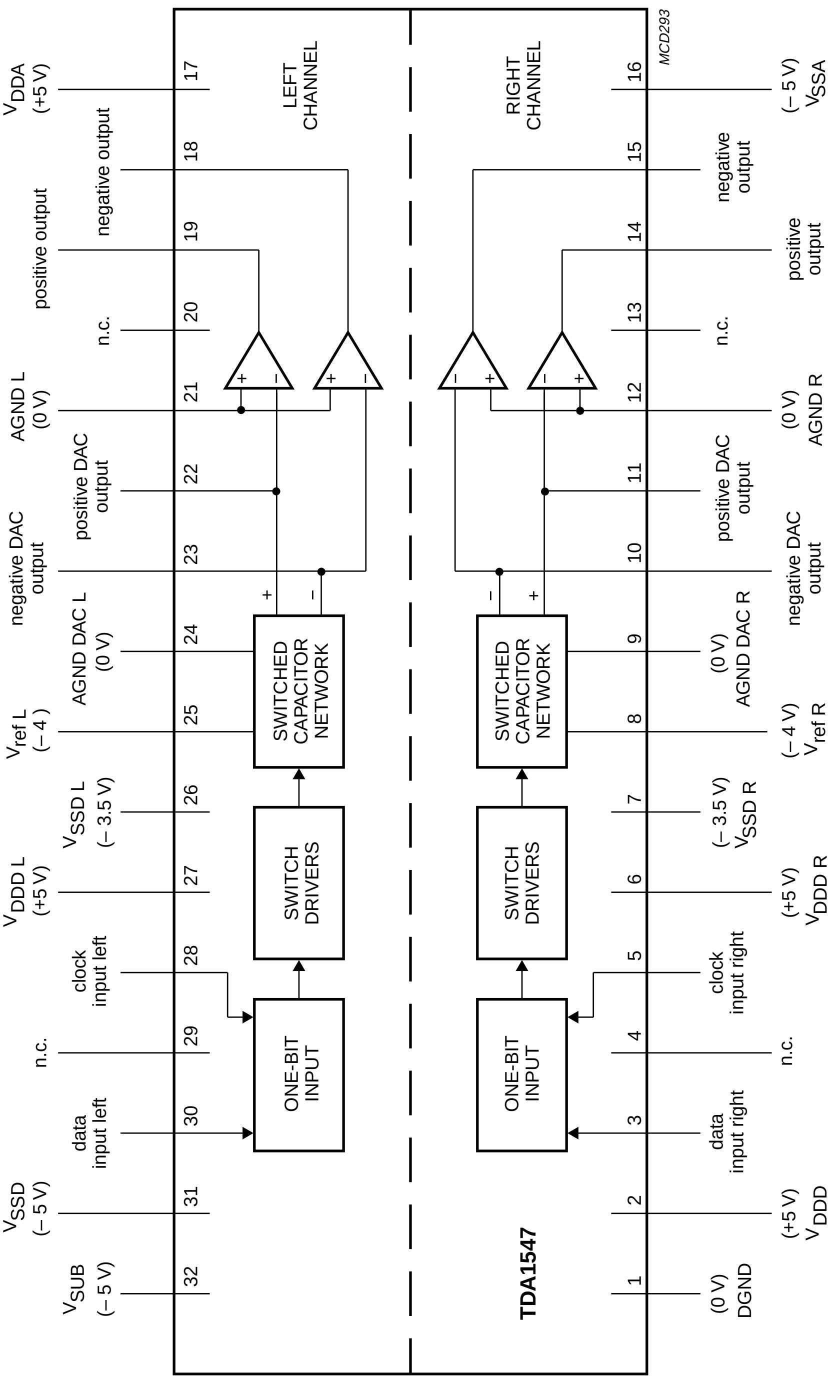


Fig.2 Block diagram.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX.	UNIT
V_{SUB}	negative substrate voltage; pin 32	note 1	–7.0	–	V
$V_{DDD\ L.\ R}$	positive digital supply voltage; pins 27 and 6		–	5.5	V
V_{DDD}	positive digital supply voltage; pin 2		–	5.5	V
$V_{SSD\ L.\ R}$	negative digital supply voltage; pins 26 and 7		–4.0	–	V
V_{SSD}	negative digital supply voltage; pin 31		–5.5	–	V
V_{DDA}	positive analog supply voltage; pin 17		–	6.0	V
V_{SSA}	negative analog supply voltage; pin 16		–6.0	–	V
$V_{DDD\ L.\ R} - V_{SSD\ L.\ R}$	supply voltage difference between pins 27, 6 and pins 26, 7		–	9.0	V
P_{tot}	total power dissipation	T_{amb} = 70 °C	–	1300	mW
$V_{ref\ L.\ R}$	input reference voltage; pins 25 and 8		–6.0		V
$V_{CLK\ L.\ R}$	input voltage clock; pins 28 and 5		–0.5	V_{DDD}+0.5	V
$V_{I\ L}$	input voltage channel; pin 30		–0.5	V_{DDD}+0.5	V
$V_{I\ R}$	input voltage channel; pin 3		–0.5	V_{DDD}+0.5	V
T_{amb}	operating ambient temperature		–20	70	°C
T_{stg}	storage temperature		–40	150	°C
T_{XTAL}	maximum crystal temperature		–	150	°C
V_{ES}	electrostatic handling	note 2	–	2000	V

Notes to the limiting values

1. The substrate voltage must be lower than or equal to the lowest supply voltage.
2. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

CHARACTERISTICS

V_{DDD}, $V_{DDD\ L.\ R}$, V_{DDA} = +5 V; V_{SSD}, V_{SSA} = –5 V, $V_{SSD\ L.\ R}$ = –3.5 V; $V_{ref\ L.\ R}$ = –4 V; T_{amb} = 25 °C; f_{CLK} = 8.46 MHz; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Supply						
V_{SUB}	negative substrate voltage; pin 32	note 1	–7.0	–	–4.5	V
$V_{DDD\ L.\ R}$	positive digital supply voltage for one channel; pins 27 and 6		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage for both channels; pin 2		4.5	5.0	5.5	V
$V_{SSD\ L.\ R}$	negative digital supply voltage for one channel; pins 26 and 7		–4.0	–3.5	–3.0	V
V_{SSD}	negative digital supply voltage for both channels; pin 31		–5.5	–5.0	–4.5	V
V_{DDA}	positive analog supply voltage; pin 17		4.5	5.0	6.0	V
V_{SSA}	negative analog supply voltage; pin 16		–6.0	–5.0	–4.5	V
$V_{DDD\ L.\ R}$ – $V_{SSD\ L,\ R}$	supply voltage difference between pins 27, 6 and pins 26, 7		–	–	9.0	V
$V_{SSD\ L.\ R}$ - V_{SSD}	supply voltage difference between pins 26, 7 and pin 31		1.3	–	–	V
$I_{DDD\ L.\ R}$	positive digital supply current for one channel; pins 27 and 6		–	0.1	–	mA
I_{DDD}	digital supply current for both channels; pin 2			29.0	46	mA
$I_{SSD\ L.\ R}$	negative digital supply current for one channel; pins 26 and 7		–	–0.1	–	mA
I_{SSD}	negative supply current for both channels; pin 31		–45	–28.0	–	mA
$–I_{DDA}$	positive analog supply current; pin 17		–	51.0	63	mA
I_{SSA}	negative analog supply current; pin 16		–63.0	–51.0	–	mA
P_{SSR1}	power supply rejection ratio	$V_{DDD\ L,\ R}$; note 6	50	–	–	dB
P_{SSR2}	power supply rejection ratio	V_{DDD}; note 6	50	–	–	dB
P_{SSR3}	power supply rejection ratio	$V_{SSD\ L,\ R}$; note 6	60	–	–	dB
P_{SSR4}	power supply rejection ratio	V_{SSD}; note 6	50	–	–	dB
P_{SSR5}	power supply rejection ratio	V_{DDA}; note 6	60	–	–	dB
P_{SSR6}	power supply rejection ratio	V_{SSA}; note 6	60	–	–	dB
P_{tot}	total power dissipation		–	800	–	mW
Clock - Input						
V_{IL}	input voltage LOW		–	–	0.5	V
V_{IH}	input voltage HIGH		4.5	–	–	V
I_{IL}	input current LOW	V_i = 0.5 V	–10	–	10	µA

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	input current HIGH	V_i = 4.5 V	–10	–	10	µA
C_i	clock input capacitance		–	5	–	pF
f_{CLK}	clock input frequency		–	–	10	MHz
Channel left/right inputs						
V_{IL}	input voltage LOW		–	–	0.5	V
V_{IH}	input voltage HIGH		–	4.5	-	V
I_{IL}	input current LOW	V_i = 0.5 V	–10	–	10	µA
I_{IH}	input current HIGH	V_i = 4.5 V	–10	–	10	µA
C_i	channel input capacitance; pins 3, 30		–	5	–	pF
V_{ref}	reference input voltage; pins 8, 25	note 2	–	–4 ±0.4	–	V
Audio outputs						
$V_{OUT(RMS)}$	output voltage (RMS value); pins 14, 19; pins 15, 18	notes 2 and 3	0.85	1.0	1.15	V
(THD + N)/S	THD + Noise; 0 dB	f = 1 kHz;	–	–101	–96	dB
		notes 3 and 4	–	0.0009	0.0016	%
(THD + N)/S	THD + Noise; 0 dB	20 Hz - 20 kHz;	–	–101	–	dB
		notes 3 and 5	–	0.0009	–	%
(THD + N)/S	THD + Noise; –20 dB	f = 1 kHz; notes 3 and 4	–	–88	–84	dB
(THD + N)/S	THD + Noise; –60 dB	f = 1 kHz; notes 3 and 4	–	–48	–44	dB
S/N	signal-to-noise ratio	pattern 0101; notes 3 and 7	109	111	–	dB
S/N	signal-to-noise ratio; “A”-weighting	pattern 0101; notes 3 and 7	–	113	–	dB
α	channel separation	f = 1 kHz	101	115	–	dB
Timing						
t_r	rise time clock input	C_L = 20 pF	–	5	10	ns
t_f	fall time clock input	C_L = 20 pF	–	5	10	ns
$t_{CLK\ L}$	clock input LOW time		45	–	–	ns
$t_{CLK\ H}$	clock input HIGH time		45	–	–	ns
t_r	channel input rise time	C_L = 20 pF	–	10	15	ns
t_f	channel input fall time	C_L = 20 pF	–	10	15	ns
t_{HD}	channel input hold time		25	–	–	ns
t_{SU}	channel input set-up time		0	–	–	ns

Notes to the characteristics

1. The substrate voltage must be lower than or to equal than the lowest supply voltage.
2. Output level tracks linearly with both the clock frequency and the reference voltage ($V_{ref\ L}$ or $V_{ref\ R}$).
3. Device measured in differential mode with external components as shown in Fig.5.
4. Measured with a one-bit data signal generated by the SAA7350 from an 8 f_s (352.8 kHz), 20-bit, 1 kHz digital sinewave. Measured over a 20 Hz to 20 kHz bandwidth.
5. Measured with a one-bit data signal generated by the SAA7350 from an 8 f_s (352.8 kHz), 20-bit, 20 Hz to 20 kHz digital sinewave. Measured over a 20 Hz to 20 kHz bandwidth.
6. Power supply rejection ratio measured with f_{ripple} = 1 kHz and v_{ripple} = 100 mV.
7. The specified signal-to-noise ratio includes noise introduced by the application components as shown in Fig.5.

TIMING

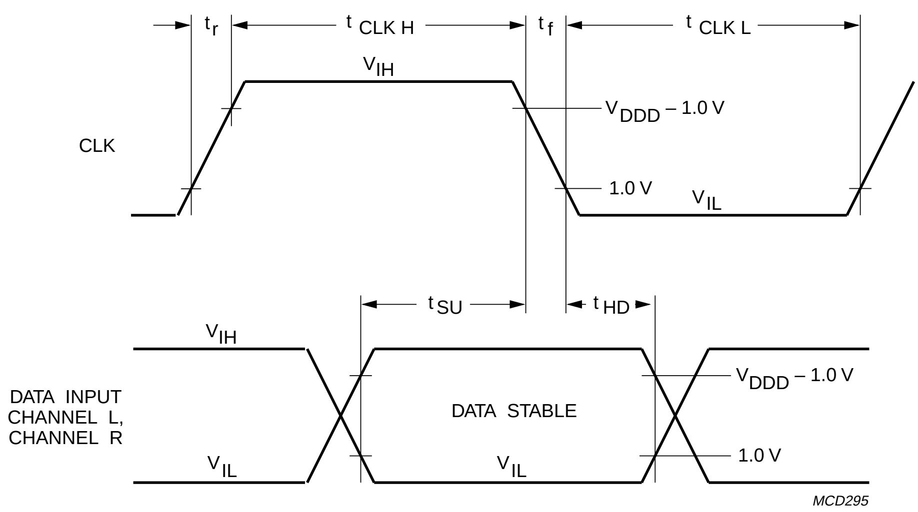


Fig.3 Timing waveform.

APPLICATION INFORMATION

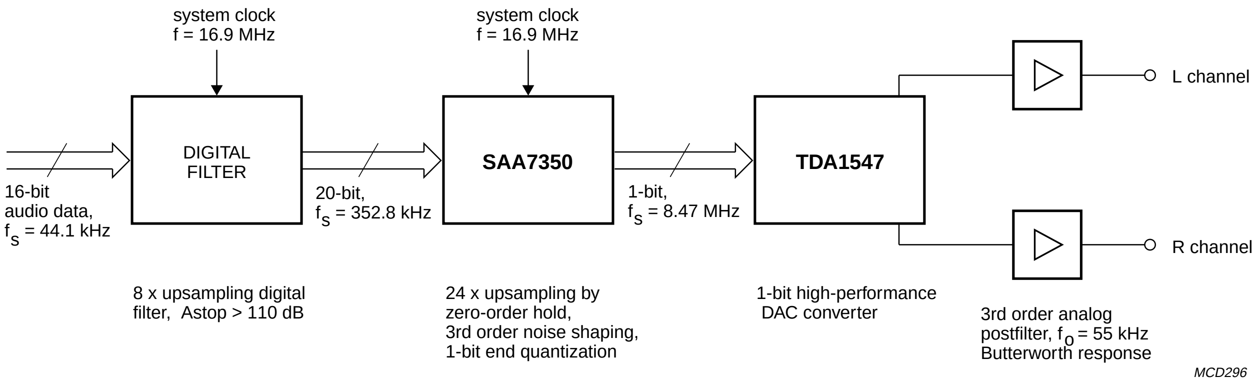


Fig.4 CD-range bitstream reconstruction system (192 f_s over-sampling).

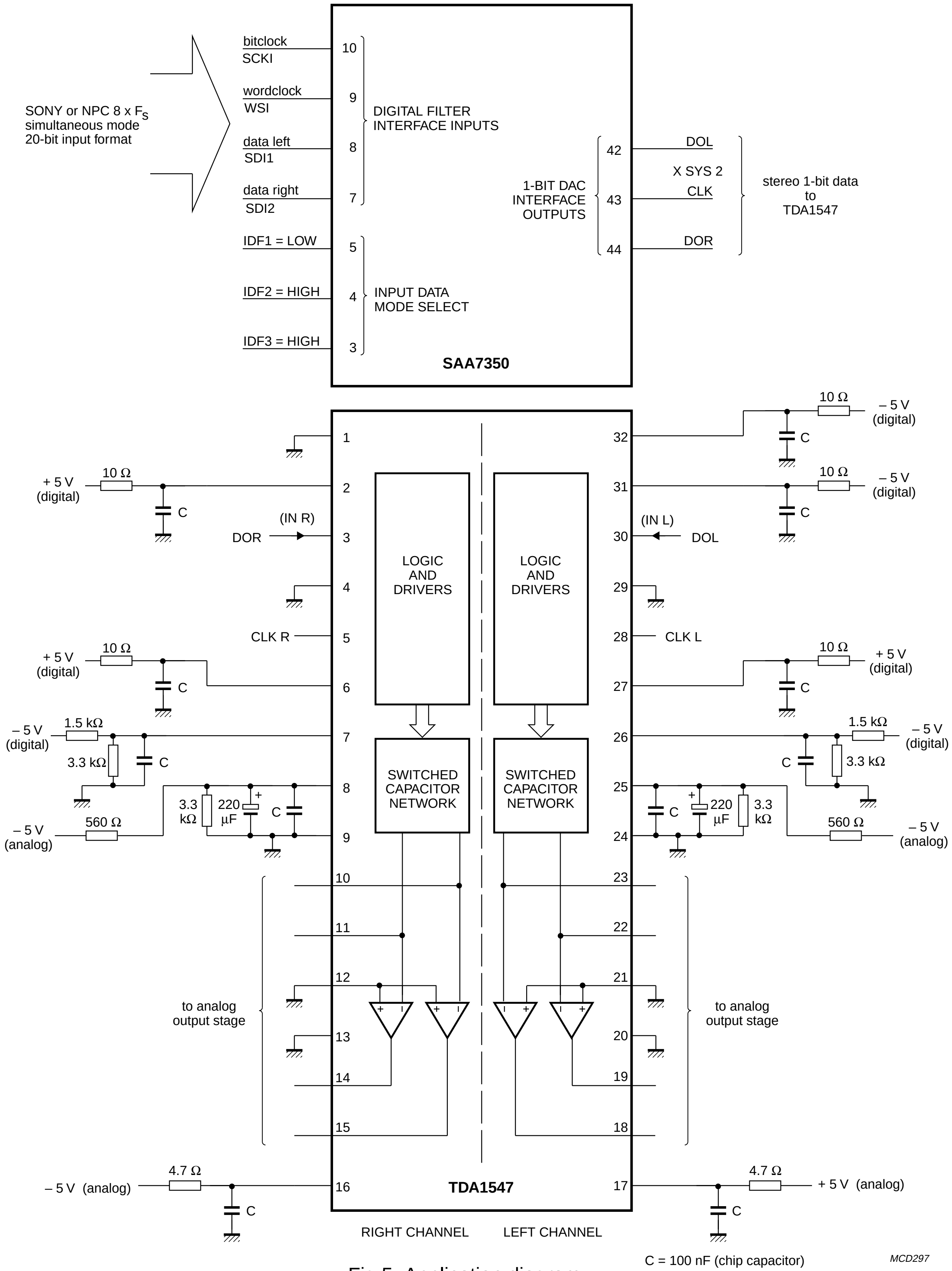


Fig.5 Application diagram.

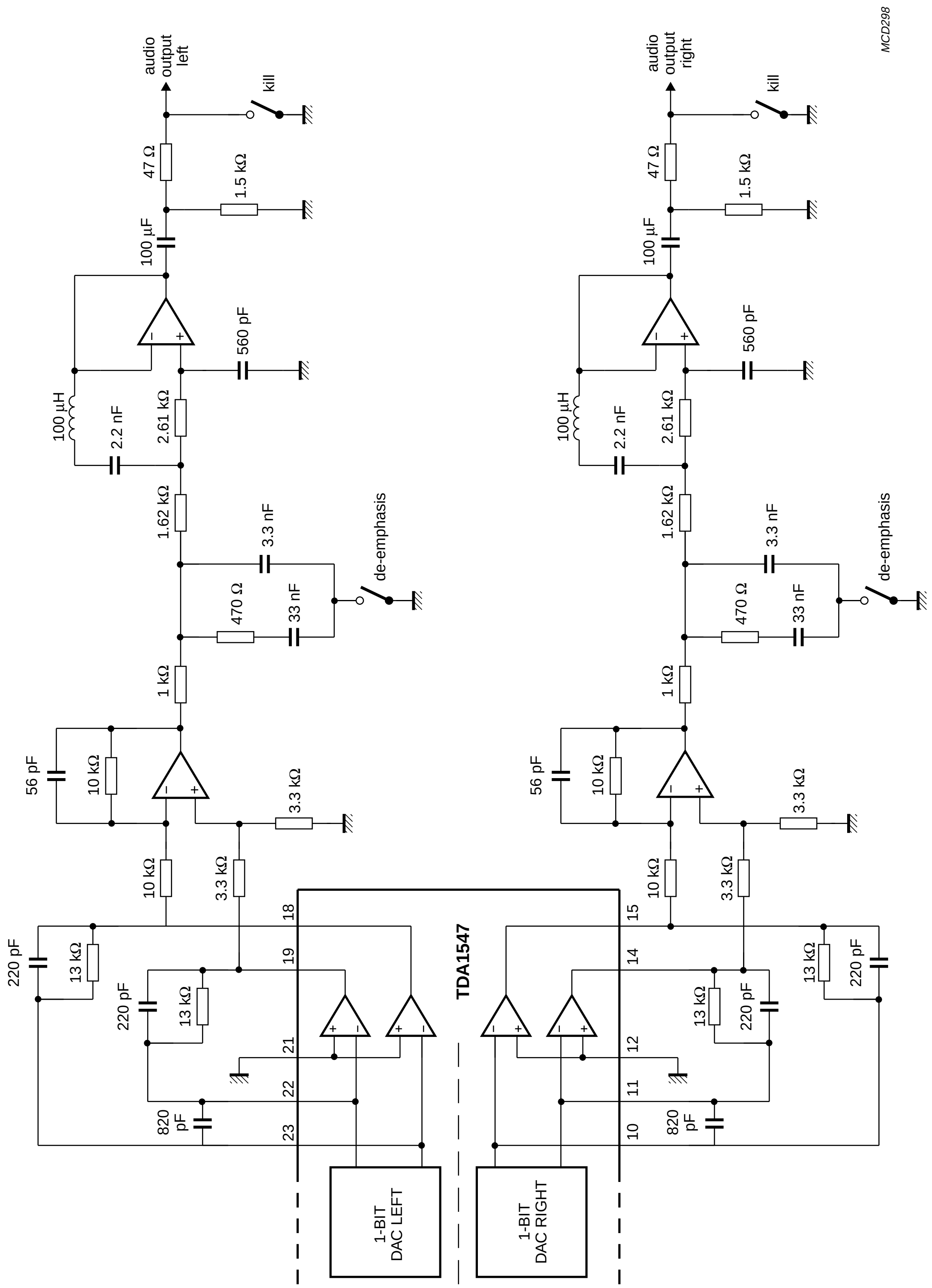


Fig.6 Post-filter for 192 f_S application (f_0 = 55 kHz).

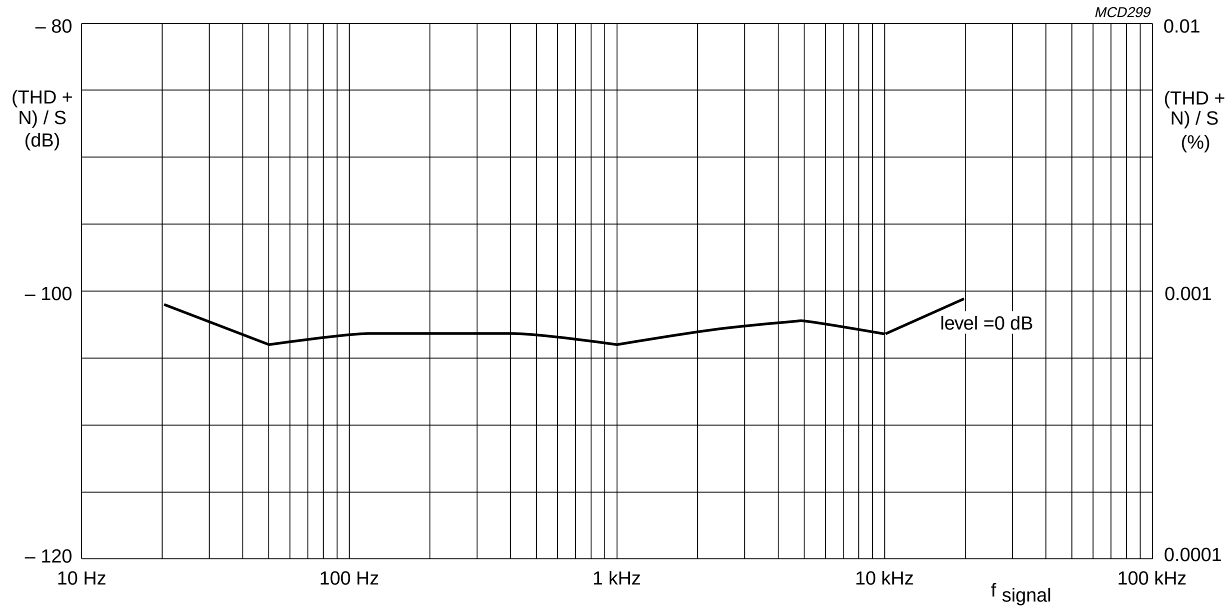


Fig.7 (THD + N)/S as a function of signal frequency.

Note: Graph constructed from average measurements values of a small amount of engineering samples. No guarantee for typical values is implied.

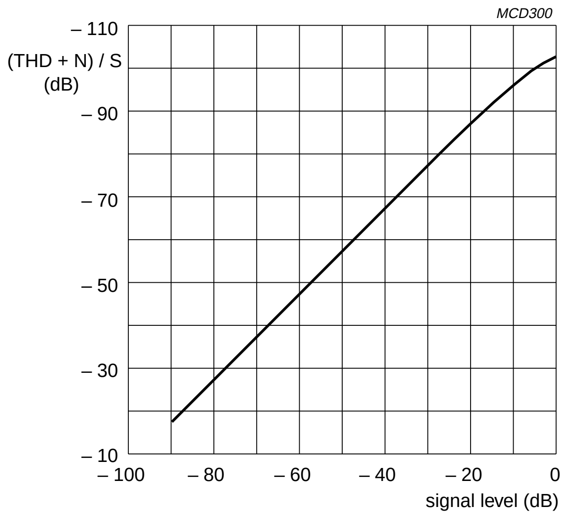


Fig.8 (THD + N)/S as a function of test signal level.

Note: Graph constructed from average measurement values of a small amount of engineering samples. No guarantee for typical values is implied.

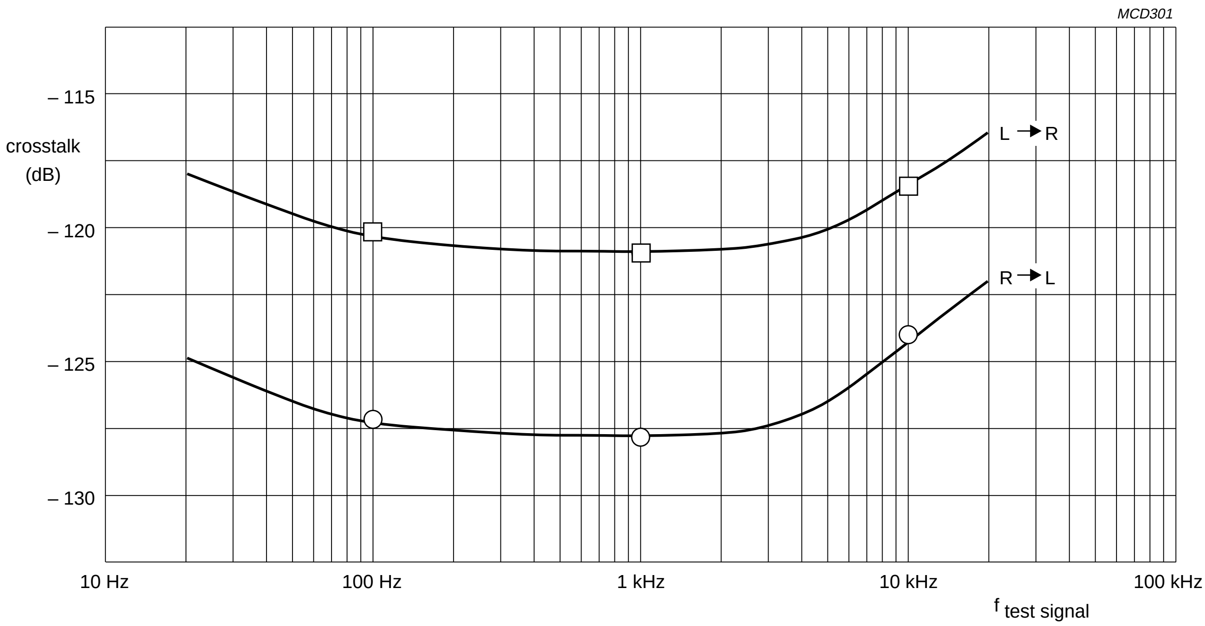
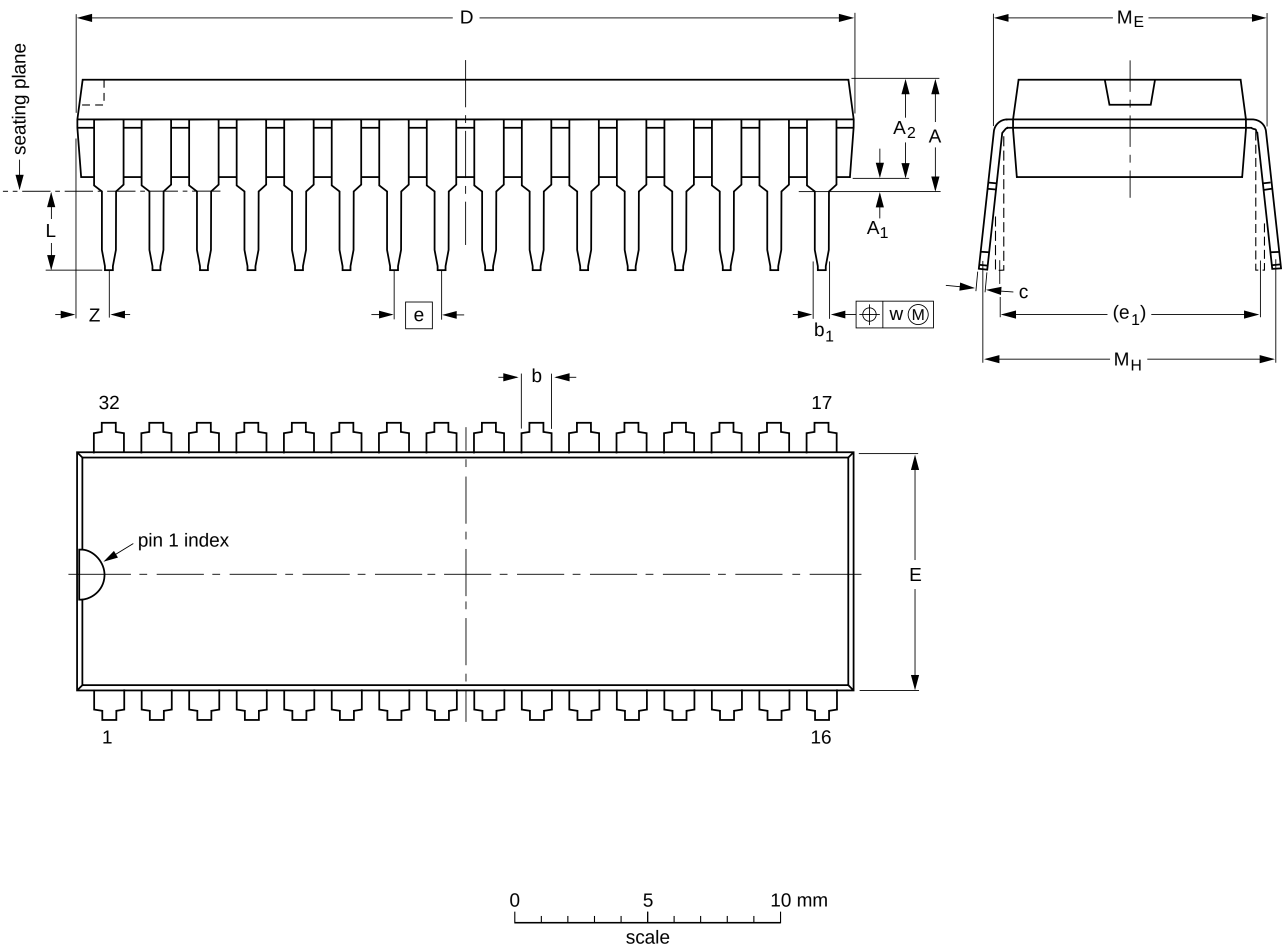


Fig.9 Inter-channel crosstalk as a function of signal frequency.

Note: Graph constructed from average measurements values of a small amount of engineering samples. No guarantee for typical values is implied.

PACKAGE OUTLINE

SDIP32: plastic shrink dual in-line package; 32 leads (400 mil) **SOT232-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.8	1.3 0.8	0.53 0.40	0.32 0.23	29.4 28.5	9.1 8.7	1.778	10.16	3.2 2.8	10.7 10.2	12.2 10.5	0.18	1.6

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT232-1						~~92-11-17~~ 95-02-04

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.